MICROSCALE PV CELLS FOR CONCENTRATED PV APPLICATIONS

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ABSTRACT: We describe a process to manufacture ultrathin photovoltaic (PV) cells from crystalline silicon and gallium arsenide. The method uses technologies developed for Microsystems and has been proven to release small form factor (< 1 mm) and ultrathin solar cells (1.15 μm thick for GaAs, and down to 14 μm in crystalline silicon) with demonstrated functionality. The 14 μm thick c-Si solar cells have achieved efficiencies in excess of 10%. The scale of these cells provide significant benefits for low, medium, and high concentration solar power. These benefits include simplified thermal management, better optical efficiency of the concentrating system, and low-cost module assembly. Due to these advantages over larger scale cells, our economic models predict that this technology could provide $\$0.50/W_{peak}$ module manufacturing costs with additional savings in the balance of system costs relative to current PV system technologies.

KEYWORDS: Thin PV cells, microsystem enabled photovoltaics, small form factor GaAs and silicon solar cells

1 INTRODUCTION

Microsystem technologies are best suited for applications where there exists a scaling benefit, such as improved performance, new functionality, or decreased cost with a decrease in system or component size. Within solar power, there are a number of significant scaling benefits associated with reducing the size (thickness as well as lateral dimensions) of solar cells. These benefits are seen at the cell, module, and system levels of solar power systems.

There have been some reports in the literature of the exploitation of PV cell scaling benefits. Some examples include the Sliver Cells developed at the Australia National University and commercialized by Origin Energy [1], similar thin and long solar cells developed at the University of Illinois [2], and the application of LED technology to PV cells pursued by the Universidad Politécnica de Madrid [3]. The cells described in these previous reports have lateral dimensions down to about 1 mm.

In this work we describe gallium arsenide and crystalline silicon (c-Si) solar cells we have developed that have lateral dimensions down to 250 μm and thickness down to 1.15 μm for GaAs and 14 μm for c-Si. These cells are fabricated on standard thickness wafers using standard tool sets and are released or lifted-off the wafers in such as way that the remaining substrate can be reused for additional processing. Cells of both materials have demonstrated photovoltaic functionality. To date we have performed some optimization of the c-Si cells and have achieved over 10% efficiencies of the cells.

2 SCALE BENEFITS OF MICROSCALE PV CELLS

The benefits to solar systems resulting from reducing the size of PV cells are seen at the cell, module, and system level of solar PV systems. This is particularly compelling since achieving grid cost parity goals requires that costs be reduced at all levels of PV systems. Some of the benefits are specific to a particular concentration range (i.e., high concentration or low concentration) or a particular material (i.e. c-Si or III-V).

At the cell level, the scale benefits allow reduced costs and improved efficiency. Specifically, the benefits seen at the cell level include:

- Reduced cell thickness and wafer reuse can significantly reduce material cost
- Backside contacts allow improved efficiency (no shading) and makes contacting the cells simpler
- Small scale cells better utilize wafer area by reducing edge exclusion area
- Cells can be hexagons which provide better area usage than squares/rectangles required by die-saw
- Small cells can be created on any size wafer while 1 cell/wafer manufacturing model currently used by c-Si manufacturers are limited in wafer size (Increased wafer size decreases processing costs/area.)
- High quality processing provided with IC fabrication tools should allow near-ideal cell performance (>20% for c-Si, > 40% for III-V multilayer cells).
- Small PV cells tend to be more efficient (until surface recombination around edge becomes significant) [3].
- Small cell dimensions allow very efficient carrier collection.

At the module level, the scaling benefits not only reduce costs and improve performance, they also introduce new functionality that is currently not available with traditional c-Si or III-V modules. The module scale benefits include

- Modules can be assembled with low-cost automated tools such as pick-and-place tools used for electronics assembly. (Assembly cost for 500 μm cells with 500X concentration and 30% module efficiency is only ~$\$0.025/W_{peak}$.)
- Modules can be assembled at even lower costs by using self-assembly concepts for small integrated circuit die currently under development [4,5].
- Since all high-temp processing is performed on the wafer, the module materials can be low-temperature, low-cost materials.
- Because of the small cell size, modules can be highly flexible *and* high-efficiency.

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- Rigid, high-efficiency modules that conform to a variety of shapes can be manufactured.
- Building Integrated PV (BIPV) panels are possible, reducing material and installation costs.
- Concentration can be performed with low-cost and optically efficient refractive microlens arrays (instead of less efficient Fresnel lenses).
- Small cell size allows short focal lengths for concentrating optics, allowing direct lamination of optics to PV cells without a cavity between.
- Micro-scale cells allow lower cell operating temperatures than macro-scale cells at the same concentration ratios (see Figure 1).

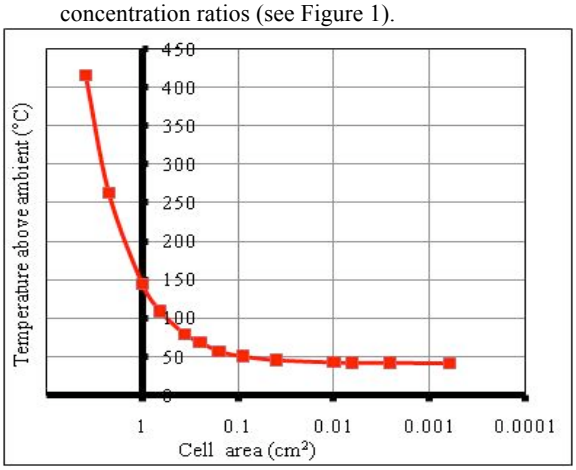

Figure 1. Finite element analysis of thermal behavior of a 500X concentrator system, cooled by convection. The figure gives the cell operating temperature above ambient for cells of decreasing size. This indicates that for cells less than about 1 mm^2, the operating temperature is essentially that of a one sun module.

At the system level, the scale benefits provide unique functionality that again result in improved efficiencies and reduced system costs. These benefits include

- High-voltage output directly from modules is possible due to the large number of cells comprising the module (eliminating the need for either DC to DC converters or thicker, more expensive system wiring).
- High-efficiency panels reduce racking and installation costs.
- Integration of health monitoring and power conditioning integrated circuits within the module using the same low-cost module assembly techniques already proposed.
- Small relative displacements between a micro-scale PV cell array and a microlens array can provide high-accuracy and high-bandwidth tracking, reducing tracking cost and complexity and provide pointing accuracy during windy conditions (due to high-speed response of tracker).
- BIPV modules reduces installation labor costs

Taken in aggregate, the impact of these benefits can be very significant for a solar PV system. Figure 2 provide an estimate of the $/W$_{peak}$ manufacturing cost of a c-Si modules manufactured using these concepts as a function of concentration. Assumptions for this model include 24% c-Si cell efficiency, 8" wafers used with a per wafer processing cost of $120/wafer, 95% yield of PV cells, 850 W/m^2 incoming direct solar power (assumes ~15% of light is diffuse), 6% light lost in optical system, assembly of module performed with self-assembly giving negligible (zero) per part assembly cost, module materials are $50/m^2, and no efficiency improvement is assumed with increased concentration. In addition to the low module costs/W$_{peak}$ provided by the small scale cells, there are additional system cost benefits not captured in this analysis that would result in an even lower overall system cost.

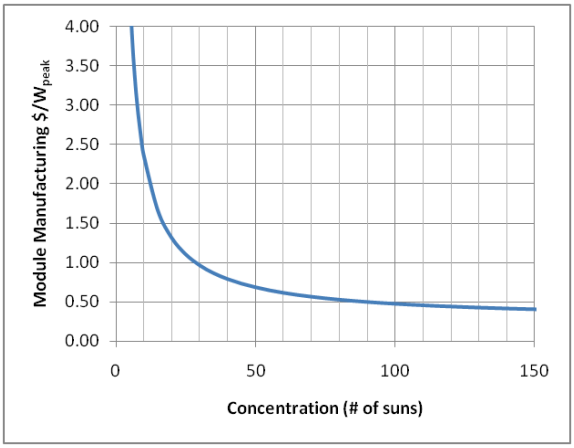

Figure 2. Predicted module production cost per peak Watt as a function of concentration.

3 MICROSCALE PV CELL FABRICATION

We have developed initial prototypes of thin, sub-mm dimensioned c-Si and III-V cells designed to take advantage of the scale benefits present in solar PV power. Figure 3 shows images of representative c-Si and III-V cells. The c-Si cell has backside contacts and is 14 µm thick. The III-V cell is a single-junction GaAs cell and is 1.15 µm thick. Both cells are 250 µm across. (We have also demonstrated 500 µm and larger cells.)

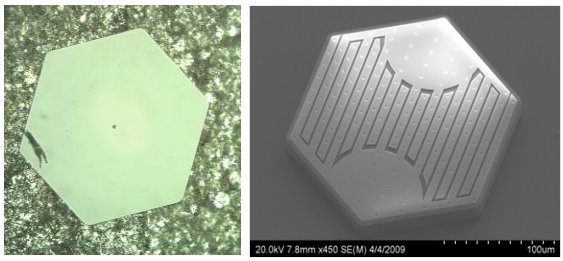

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Figure 3. (A) 1.15 µm thick single-junction GaAs cell. (B) 14 µm thick back-contact c-Si cell. Both cells are 250 µm wide.

These cells are fabricated on standard thickness wafers using standard microfabrication tools, followed by a lift-off process that leaves the remaining wafer available for processing additional PV cells.

2.1 GaAs cells

The GaAs cells are fabricated using epitaxial lift-off concepts. Unlike the typical method of creating epitaxial lift-off cells, these are created without using a protective wax material, or a film transfer substrate. To create the prototype device, an aluminum arsenide (0.1µm)

sacrificial layer is grown on a handle wafer, followed by a very simple GaAs cell. The cell is comprised of a *n*+ GaAs layer, a *p* GaAs layer, and a *p*+GaAs layer as shown in Figure 4.

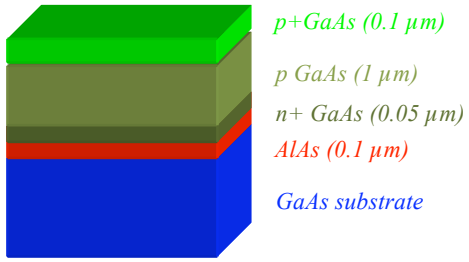

Figure 4.Material layers for the GaAs prototype cell.

Once the stack is complete, the individual cells are metalized on the backside by a metal lift-off process with sputtered gold. Etch release holes and the sidewalls of the cells are created by etching between the cells using lithography and a reactive ion etch (RIE). The etch goes through the GaAs cell structure to the AlAs layer. The sacrificial layer is then selectively etched with 49% HF in water with Tergitol added. Compared to full wafer epitaxial lift-off (required when wax or a receiving substrate is used) which has release times as long as two to three days, we have seen release times as short as 10 minutes. The GaAs wafer that remains after release can be reused to grow and release additional cells. Figure 5 illustrates the cell processing and lift off procedure

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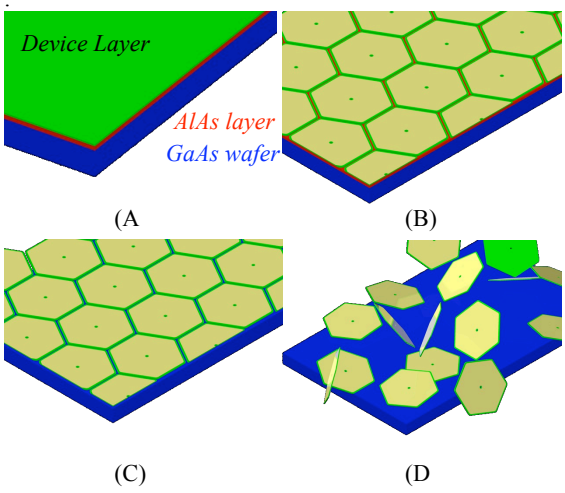

Figure 5. (A) sacrificial layer and GaAs cell layers are grown. (B) metallization through gold lift-off (C)etching of the cell sidewalls and etch release holes (D) selective wet etching of the AlAs release layer and lift-off of the PV cells.

2.1 Silicon cells

Prototype c-Si cells have been fabricated in two ways. The first approach uses a silicon on insulator (SOI) wafer with the cells released through a selective HF etch of the buried oxide layer. The SOI wafers have a 20 µm device layer on top of a 1µm buried oxide layer. We have demonstrated PV cells with lateral dimensions of 250 µm through 1 cm and thicknesses of 20 µm. After lifting off the PV cells, the remaining wafer can be reprocessed through either a SIMOX like process or through a bond and cleave process.

The second method takes advantage of the silicon crystal plane selectivity of KOH. This method requires a (111) oriented silicon wafer. We have demonstrated lift-off of 14 μm thick, 250 μm and 500 μm c-Si PV cells with this technique. A silicon nitride film is required on the sidewalls of the cell to protect the cell during the KOH etch. The film also acts to passivate the sidewall.

We have tested different methods to create the junction in the PV cells including solid-source diffusion, implantation, and spin-on-dopants. Once the junction is created, a metallization step is performed. We have explored using both aluminum and tungsten with a titanium silicide contact with the silicon. After the metallization, the cell sidewalls are defined by photolithography and deep reactive ion etching (DRIE) to the depth desired.

With the cell sidewalls defined the cells are released either with HF for the SOI approach or KOH for the (111) silicon approach.

We have explored some techniques for creating passivating films on the released silicon surface. The techniques we have explored to date include ALD alumina, LPCVD silicon oxide, and LPCVD silicon nitride. We have achieve cell efficiencies in excess of 10%.

A more detailed analysis of the c-Si PV cell fabrication process can be found in [6].

4. CONCLUSIONS

We have demonstrated functional prototype PV cells of c-Si and GaAs. These cells have lateral dimensions of between 250 µm and 1 cm and are 14 to 20 µm thick for c-Si and are between 1.15 and 5 µm thick for GaAs. By significantly decreasing the size of PV cells, a number of scaling benefits are introduced that increase performance, decrease cost, and provide unique functionality. The scaling benefits are seen at all levels of solar PV systems (cell, module, and system).

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